

## ABSTRACT

A memory cell array employs a memory element as a memory cell. The memory element is constructed of a gate electrode formed via a gate insulation film on a 5 semiconductor layer, a channel region arranged under the gate electrode, diffusion regions that are arranged on both sides of the channel region and have a conductive type opposite to that of the channel region, and memory function bodies that are arranged on both sides of the gate 10 electrode and have a function to retain electric charges. When first and second power voltages VCC1 and VCC2 supplied from the outside are lower than a prescribed voltage, a rewrite command to a memory circuit 34 that includes the memory cell array is inhibited by a lockout circuit 33a. 15 With this arrangement, there are provided a semiconductor storage device capable of achieving storage retainment of two bits or more per memory element and stable operation even if the device is miniaturized and preventing the occurrence of a malfunction of rewrite error and so on 20 attributed to a reduction in the power voltage supplied from the outside and a control method therefor.